IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Huy Thanh Vo	Examiner: Mai, Son Luu
Serial No.:	09/808,750	Group Art Unit: 2827
Filed:	March 15, 2001	Docket No.: 303.723US1
Title:	DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR MEMORY DEVICES	

REPLY BRIEF UNDER 37 CFR § 41.41

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Commissioner for Patents
P.O. Box 1450
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This Reply is presented in response to the Examiner's Answer, (hereinafter the "Answer") dated January 5, 2006, which was sent in answer to Appellant's Appeal Brief, filed on October 9, 2006. Appellant's Appeal Brief was filed in response to the rejection of claims 1-41 and 45-57 of the above-identified application.

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Argument

The Appellant has reviewed the Answer, and believes the statements in the original Appeal Brief remain accurate and compelling. In responding to the Answer, the Appellant wishes to further clarify certain points of distinction between the pending claims and the cited references in response to newly presented comments. The corresponding pages of the Answer will be used to reference each of these points.

In addition, Appellant maintains each and every argument submitted in Appellant's pending Appeal Brief, and respectfully submits that each of the arguments are proper and valid in view of all of the statements made in the Answer. Therefore, any lack of reference in this Reply Brief to a particular argument in the pending Appeal Brief is not to be construed as an admission that the Appellant agrees with any of the statements in the Answer (Examiner's Answer). Appellant asks that the statements made in Appellant's pending Appeal Brief be considered in full, in addition to the statements included with this Reply Brief.

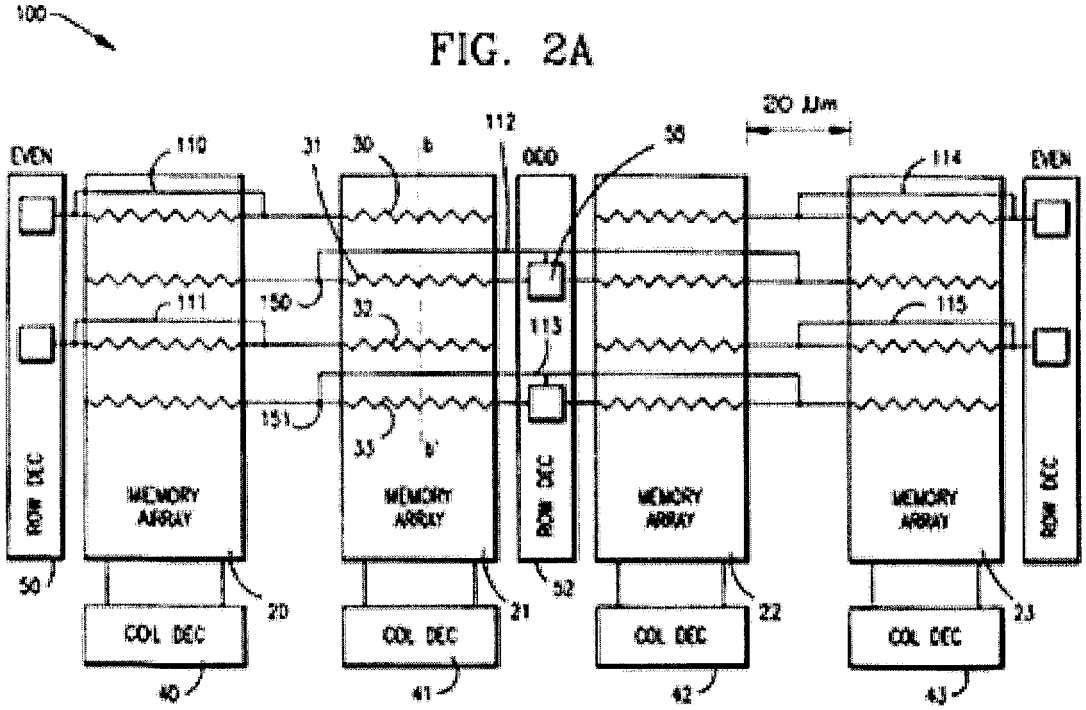
Reply to Examiner's Answer (10) Response to Argument

As stated in Appellant's Appeal Brief, a proper *prima facie* showing of anticipation under 35 U.S.C. § 102(b) has not been shown because Cowles fails to teach each and every element of claims 1-41 and 45-57. To anticipate a claim, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Cowles does not meet this legal standard of anticipation.

As stated in the Appeal Brief, Appellant cannot find in Cowles a strapping line that bypasses only a portion of a wordline within the single array, as recited in claim 1 and similarly recited in the other independent claims.

The Answer states throughout the rejections to claims 1-41 and 45-54 that the Examiner considers the *individual* arrays 20, 21, 22, 23 in Figure 2A of Cowles as a single array (*see* e.g., pg. 19 of the Answer).

FIG. 2A



However, the memory bank 100 of Cowles is made of more than one memory array (*see* reproduced FIG. 2A above). Cowles clearly labels *each* of the *individual* memory arrays in the Figure. Cowles also states that the invention ... may be used with any number of arrays greater than one (*see* col. 3 lines 23-27). Cowles states further that "[s]traps 112, 113 are connected to wordlines 31, 33 respectively outside the edge of [memory] array 21 as shown in FIG. 2A at nodes 150, 151 through a contact hole in the poly layers" (*see* Cowles, col. 4 lines 2-4). Cowles states further still that a respective column decoder 40, 41, 42, 43 is provided for each array 20-23 to access the particular column desired (*see* col. 3 lines 31-33).

Additionally, note that Figure 2A shows two separate even row decoders and only one odd decoder. If the individual memory arrays 20, 21, 22, 23 were a single array as urged by the Examiner, then two even row decoders would be provided to the same memory array. However, if the Examiner's interpretation of the plurality of individual arrays being a single array is correct (which Applicant does not concede), then there would be no need for the second even row decoder as shown in Cowles. Therefore, memory arrays 20, 21, 22, 23 are not a single memory array in Cowles. As a result, Cowles does not show the identical invention recited in claim 1.

In regard to the rejection to claims 55-57, Appellant cannot find in Cowles:

> a number of strapping lines ... wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder,

as recited in claim 55-57. The Answer states that, regard to claims 55-57 the Examiner now considers arrays 20-21 in Figure 2A of Cowles as a single array (*see* e.g., pg. 29 of the Answer). However, as discussed above the memory bank 100 of Cowles is made of more than one memory array. Also, note that each memory array 20, 21 includes a column decoder. If the individual memory arrays 20, 21 were a single array as urged by the Examiner, Cowles then would not teach a single column decoder connected to the memory array as recited in claim 55. Moreover, memory arrays 20, 21 of Cowles are not a single memory array. Based at least on the preceding Cowles does not show the identical invention recited in claim 55.

CONCLUSION

For the reasons stated above and in the Appellant's Appeal Brief, Appellant respectfully submits that claims 1-41 and 45-57 were not properly rejected under 35 U.S.C. § 102(b) as being unpatentable over Cowles (U.S. Pat. No. 5,940,315).

Reversal of the rejections and allowance of all pending claims is respectfully requested.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of September, 2006.

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